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Application of

Applicant	:	Joseph M. Brand
Serial No.	:	09/335,618
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Examiner	:	Alonzo Chambliss
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Assistant Commissioner for Patents
Washington, D.C. 20231

CERTIFICATE OF FACSIMILE TRANSMISSION
I hereby certify that this correspondence is being facsimile transmitted to the Patent and Trademark Office ((703) 308-7724) on January 17, 2002.

William A. Jividen — 42,695 Reg. No.

Sir:

AMENDMENT

This paper is being filed in response to the Office Action mailed December 14, 2001, thereby having a non-fee response date of no later than March 14, 2002. Reconsideration and reexamination are respectfully requested in light of the amendments and remarks below.

In the Claims

The entire set of presently pending claims has been reproduced below for the convenience of the Examiner. Amended claims are indicated as such in the parenthetical following each claim number.

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1. (Amended) A packaged semiconductor device consisting essentially of:

a semiconductor die;

a laminate defining first and second major faces, said laminate including

an electrically conductive layer,

an underlying substrate supporting said electrically conductive layer, and

E1

E1

at least one void formed in said laminate so as to extend from said first major face through said electrically conductive layer, through said underlying substrate and through said second major face; and

an encapsulant positioned to mechanically couple both said encapsulant and said semiconductor die to said first major surface of said laminate, wherein said encapsulant is further positioned to extend through said void from said first major face to said second major face and contacting said underlying substrate.

4. A packaged semiconductor device as claimed in claim 1 wherein said contact between said encapsulant and said underlying substrate is characterized by an adhesive bond.

5. A packaged semiconductor device as claimed in claim 1 wherein said encapsulant occupies substantially all of said void.

6. A packaged semiconductor device as claimed in claim 1 wherein said semiconductor die is supported by said laminate and wherein said encapsulant and said laminate are arranged to enclose substantially all of said semiconductor chip.

E2

7. (Amended) A packaged semiconductor device consisting essentially of:

a semiconductor die;

a laminate defining first and second major faces, said laminate including

a solder resist layer,

an underlying substrate,

an electrically conductive layer interposed between said solder resist layer and said underlying substrate, and

at least one void formed in said laminate so as to extend from said first major face through said solder resist layer, through said electrically conductive layer, through said underlying substrate and through said second major face; and

an encapsulant positioned to mechanically couple both said encapsulant and said semiconductor die to said first major face of said laminate, wherein said encapsulant is further positioned to extend into said void so as to contact said underlying substrate.

8. (Amended) A packaged semiconductor device consisting essentially of:

a semiconductor die;

a laminate defining first and second major faces and including a plurality of laminated layers, said laminate including at least one void formed therein so as to extend from one of said major faces through a plurality of said laminated layers; and

an encapsulant positioned to mechanically couple both said encapsulant and said semiconductor die to said first major face of said laminate, wherein said encapsulant is further positioned to extend into said void across said plurality of laminated layers so as to contact a portion of said laminate between said first and second major faces of said laminate.

9. A packaged semiconductor device as claimed in claim 8 wherein said at least one void extends from said first major face through said laminate to said second major face and wherein said encapsulant is positioned to extend through said void from said first major face to said second major face.

10. A packaged semiconductor device as claimed in claim 8 wherein said contact between said encapsulant and said laminate is characterized by an adhesive bond.

11. A packaged semiconductor device as claimed in claim 8 wherein said encapsulant occupies substantially all of said void.

12. A packaged semiconductor device as claimed in claim 8 wherein said semiconductor die is supported by said laminate and wherein said encapsulant and said laminate are arranged to enclose substantially all of said semiconductor die.

13. (Amended) A packaged semiconductor device consisting essentially of:

a semiconductor die;

E3 an epoxy resin glass-cloth laminate defining first and second major faces and including a plurality of laminated epoxy layers, said epoxy laminate including at least one void formed therein so as to extend from one of said major faces through a plurality of said laminated epoxy layers; and

an encapsulant positioned to mechanically couple both said encapsulant and said semiconductor die to said first major face of said epoxy resin glass-cloth laminate, wherein said encapsulant is further positioned to extend into said void across said plurality of laminated epoxy layers so as to contact a portion of said laminate between said first and second major faces of said laminate.

23. (Amended) A computer including at least one packaged semiconductor device consisting essential of:

E4 a semiconductor die;

a laminate defining first and second major faces, said laminate including

an electrically conductive layer,

an underlying substrate supporting said electrically conductive layer,

at least one void formed in said laminate so as to extend from said first major face through said electrically conductive layer, through said underlying substrate, and through said second major face; and

an encapsulant positioned to mechanically couple both said encapsulant and said semiconductor die to said first major face of said laminate, wherein said encapsulant is further positioned to extend into said void so as to contact said underlying substrate.

32. (Amended) A packaged semiconductor device consisting essentially of:

E5 a laminate defining first and second major faces and including a plurality of laminated layers, said laminate including at least one void formed therein so as to extend from one of said major faces through a plurality of said laminated layers;

a semiconductor chip positioned adjacent one of said major faces of said laminate; and

an encapsulant positioned to mechanically couple both said encapsulant and said semiconductor die to said first major face of said laminate, wherein said encapsulant is further positioned to extend into said void across said plurality of laminated layers so as to contact a portion of said laminate between said first and second major faces of said laminate.

33. (Amended) An encapsulated integrated circuit consisting essentially of:

E5

a printed circuit board comprises a laminate defining first and second major faces, said laminate including

a solder resist layer,

an underlying substrate,

an electrically conductive layer interposed between said solder resist layer and said underlying substrate, and

at least one void formed in said printed circuit board so as to extend from one of said major faces through said solder resist layer and said electrically conductive layer at least as far as said underlying substrate;

a semiconductor die positioned adjacent one of said major faces of said printed circuit board and being electrically conductive with said printed circuit board; and

an encapsulant positioned to mechanically couple both said encapsulant and said semiconductor die to said printed circuit board, wherein said encapsulant is further positioned to extend into said void.

34. (Amended) An encapsulated integrated circuit consisting essentially of:

a printed circuit board comprises a laminate defining first and second major faces, said laminate including a solder resist layer, a resin laminate having at least one selected layer and at least one adjacent laminated layer, and an electrically conductive layer interposed between said solder resist layer and said resin laminate, said laminate includes at least one void formed therein so as to extend from one of said major faces through said

solder resist layer and said electrically conductive layer at least as far as said adjacent laminated layer;

a semiconductor die positioned adjacent one of said major faces of said printed circuit board and being electrically conductive with said printed circuit board; and

an encapsulant positioned to substantially cover and mechanically couple both said encapsulant and said semiconductor die to said printed circuit board, wherein said encapsulant is further positioned to extend into said void so as to form an adhesive bond with at least said resin laminate.

REMARKS

Attached hereto as Appendix A is a marked-up reproduction of the changes made to the claims by the current amendments. Additions have been underscored and deletions have been bracketed.

The Examiner rejected claims 1, 4-6, 8-12, 23, and 32 under 35 U.S.C. § 102(b) as being anticipated by Hegel (U.S. 5,255,157). Additionally, the Examiner rejected claims 7, 33, and 34 under 35 U.S.C. § 103(a) as being unpatentable over Hegel as applied to claim 1, and further in view of Juskey et al. (U.S. 5,336,931). Furthermore, the Examiner rejected claims 13 under 35 U.S.C. § 103(a) as being unpatentable over Hegel as applied to claim 1, and further in view of Papathomas (U.S. 5,623,006).

Hegel teaches after conventionally bonding or mounting the semiconductor device in place to the substrate that the assembly is completed by transferring the thermoset molded plastic layer (the encapsulant) to complete the package. See column 3, lines 3-15, lines 45-48, and column 4, lines 2-7. The encapsulant therefore covers the mounted semiconductor die, wherein the formation of the plastic pillars only lock the encapsulant to the substrate. See column 3, lines 11-15, and column 4, lines 20-23. Hegel states that the purpose of the pillars is to minimize any tendency of the plastic encapsulant to separate from the PW board or the semiconductor device as a result of flexure. See column 4, lines 23-26.

Juskey et al teach the use of an adhesive 120 to attach a die 130 to the upper surface of a substrate 160, see Fig. 2. Accordingly, there is no motivation provided by

Hegel in view of Juskey et al of using an encapsulant to mechanically couple both the encapsulant and semiconductor die to the laminate without first conventionally mounting the semiconductor to the substrate.

Papathomas (US 5,623,006) teaches first joining an integrated semiconductor device 1 to a carrier substrate 2 by solder bumps 3 mated to pads 4, and then providing the encapsulant 7, see column 4, lines 1-13. Therefore, there is no motivation provided by Hegel in view of Papathomas having an encapsulant provided to mechanically couple both the encapsulant and semiconductor die to a substrate without first conventionally mounting the semiconductor to the substrate.

Further, Applicant asserts that in view of the disclosures of Juskey et al and Papathomas, one skilled in the art is reasonably lead to believe that soldering and bonding with an adhesive are the known conventional methods of mounting the semiconductor to the substrate as referred by Hegel, which all cited references disclose doing before pouring the encapsulant. Therefore, unlike the present invention, Hegel, Juskey et al, and Papathomas individual or taken together, fail to disclose or suggest using the encapsulation to mechanically couple both the encapsulant and the semiconductor die to the substrate without first conventionally mounting the semiconductor to the substrate.

Accordingly, Applicant amends the claims to recite that the claimed invention *consists essentially of* the recited features of the claims and further refines the claims by reciting that the encapsulant is positioned to mechanically couple *both* the encapsulant and the semiconductor to the substrate. Support for these amendments is provided for by the specification and drawings, thus no new matter has been entered. None of the cited prior discloses or suggests, explicitly or impliedly, the use of an encapsulant in this manner.

As pointed out in previous responses, the arguments of which are all reinstated and incorporated herein by reference, all the cited prior art require first that the semiconductor die be first conventionally mounted or bonded to the substrate, such as by solder or an adhesive, wherein the encapsulant is then applied only as a protective cover for the stated purposes. As in the present invention, the use of either solder or an

adhesive to conventionally mount or bond the semiconductor to the substrate as stated in the cited prior art would materially affect the basic and novel characteristic of the claimed invention. Mounting or bonding the semiconductor to the substrate by one of the conventionally known methods of the cited prior art, such as by solder or an adhesive, requires extra processing time and increases manufacturing costs.

CONCLUSION

The Applicant respectfully submits that, in view of the above amendments and remarks, the application is now in condition for allowance. The Examiner is encouraged to contact the undersigned to resolve efficiently any formal matters or to discuss any aspects of the application or of this response. Otherwise, early notification of allowable subject matter is respectfully solicited.

Respectfully submitted,
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